Fig. 1

(RELATED ART)

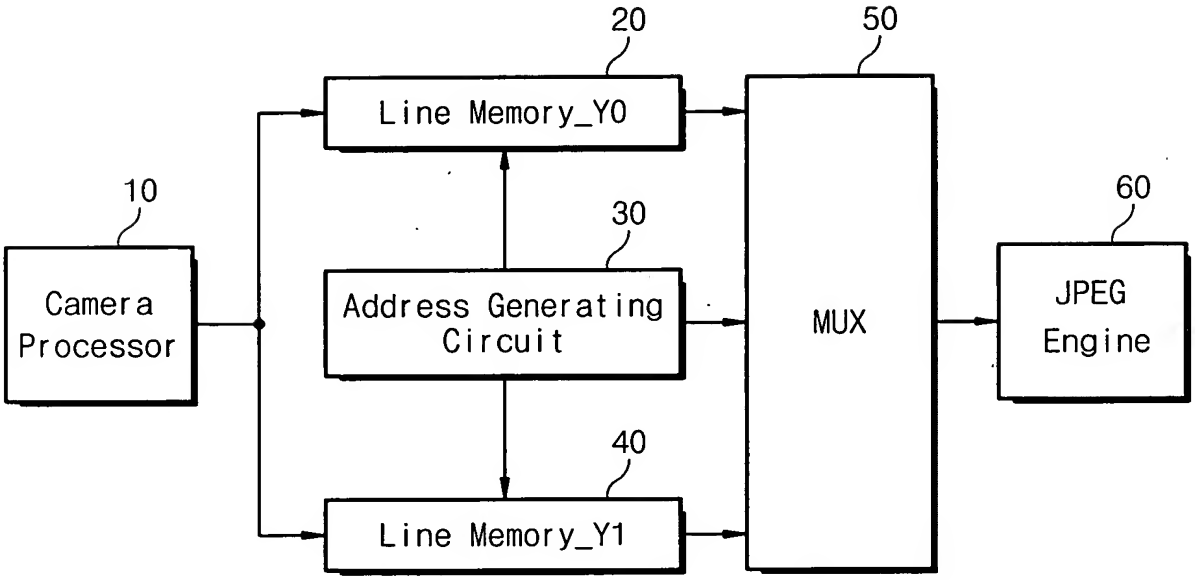

Fig. 2

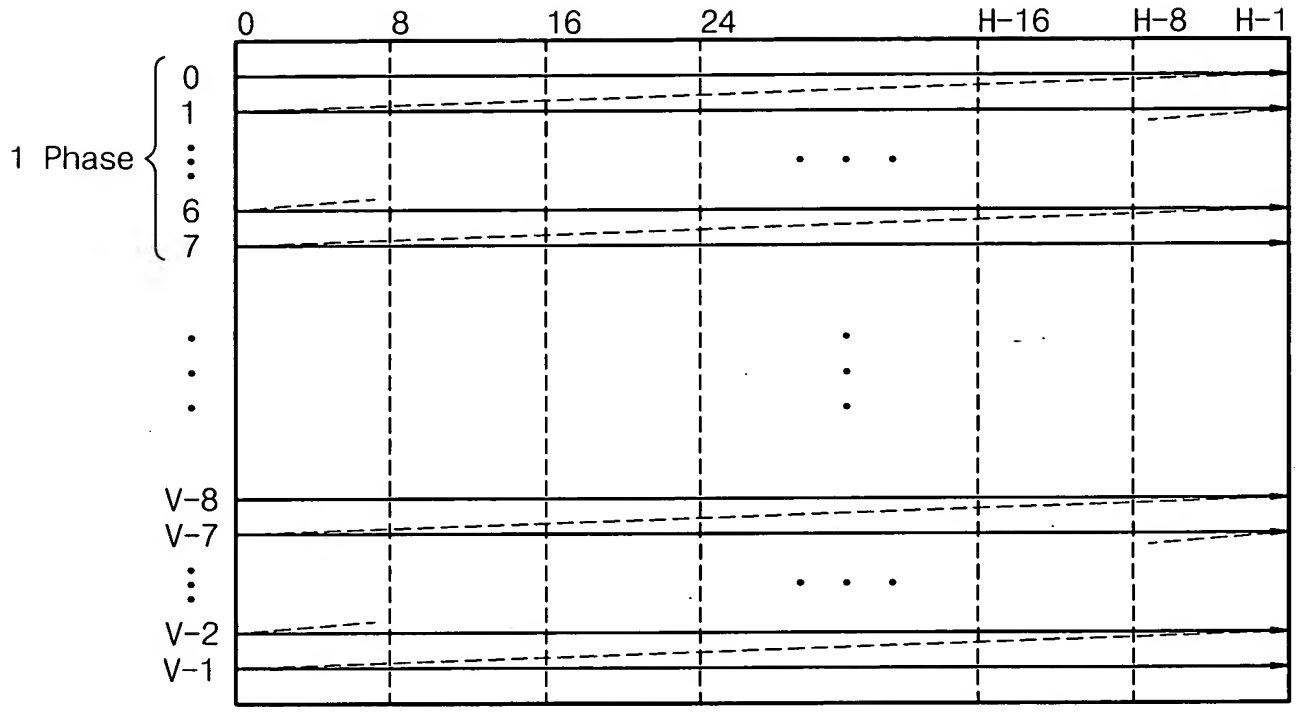

Fig. 3

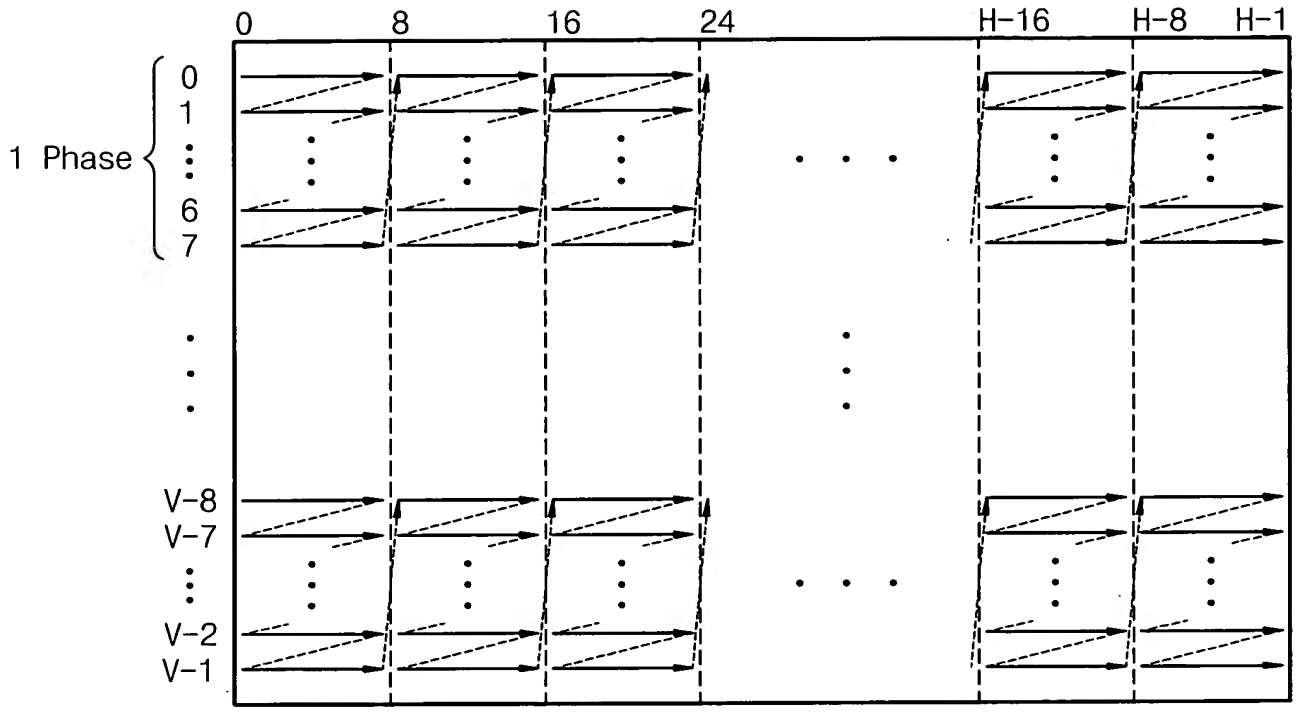

Fig. 4

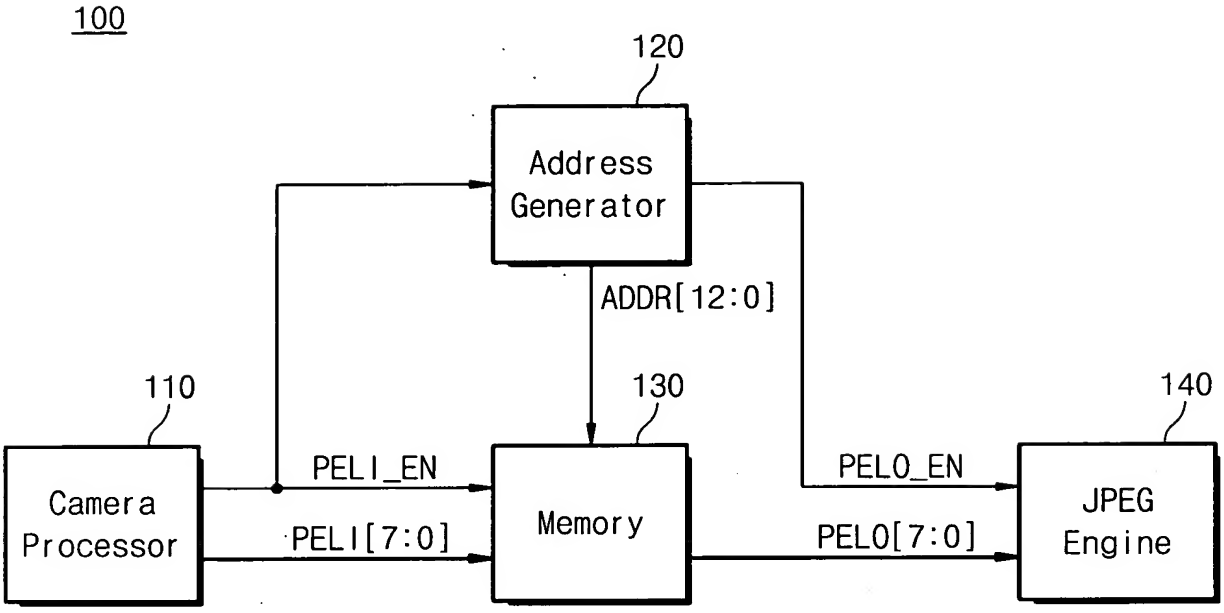
100
120
Address Generator
ADDR[12:0]
110
130
140
Camera Processor
PELI_EN
PELI[7:0]
Memory
PELO_EN
PELO[7:0]
JPEG Engine

Fig. 5

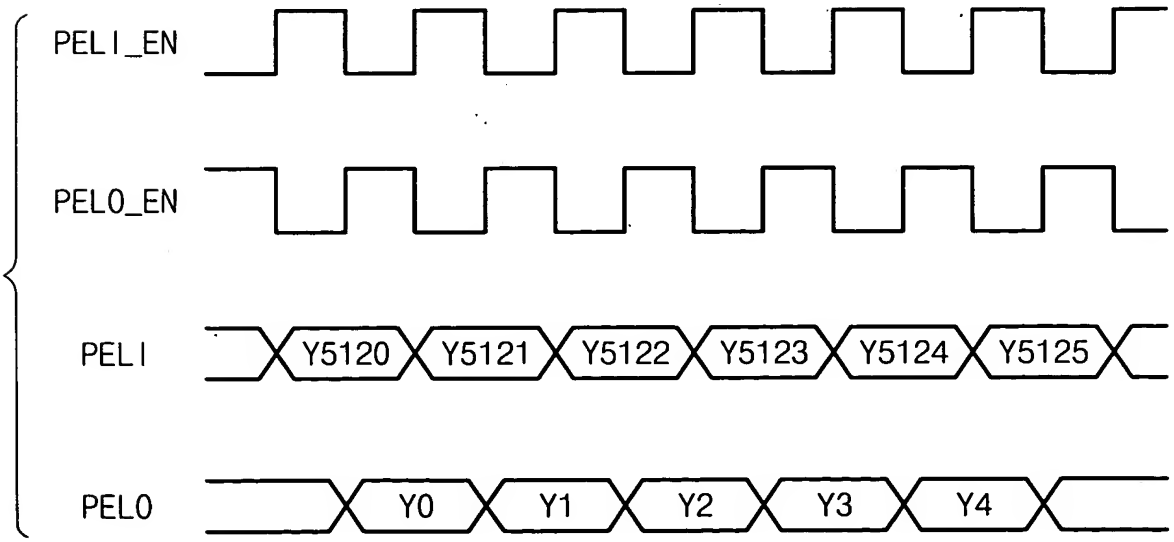
PELI_EN
PELO_EN
PELI
Y5120
Y5121
Y5122
Y5123
Y5124
Y5125
PELO
Y0
Y1
Y2
Y3
Y4

Fig. 6

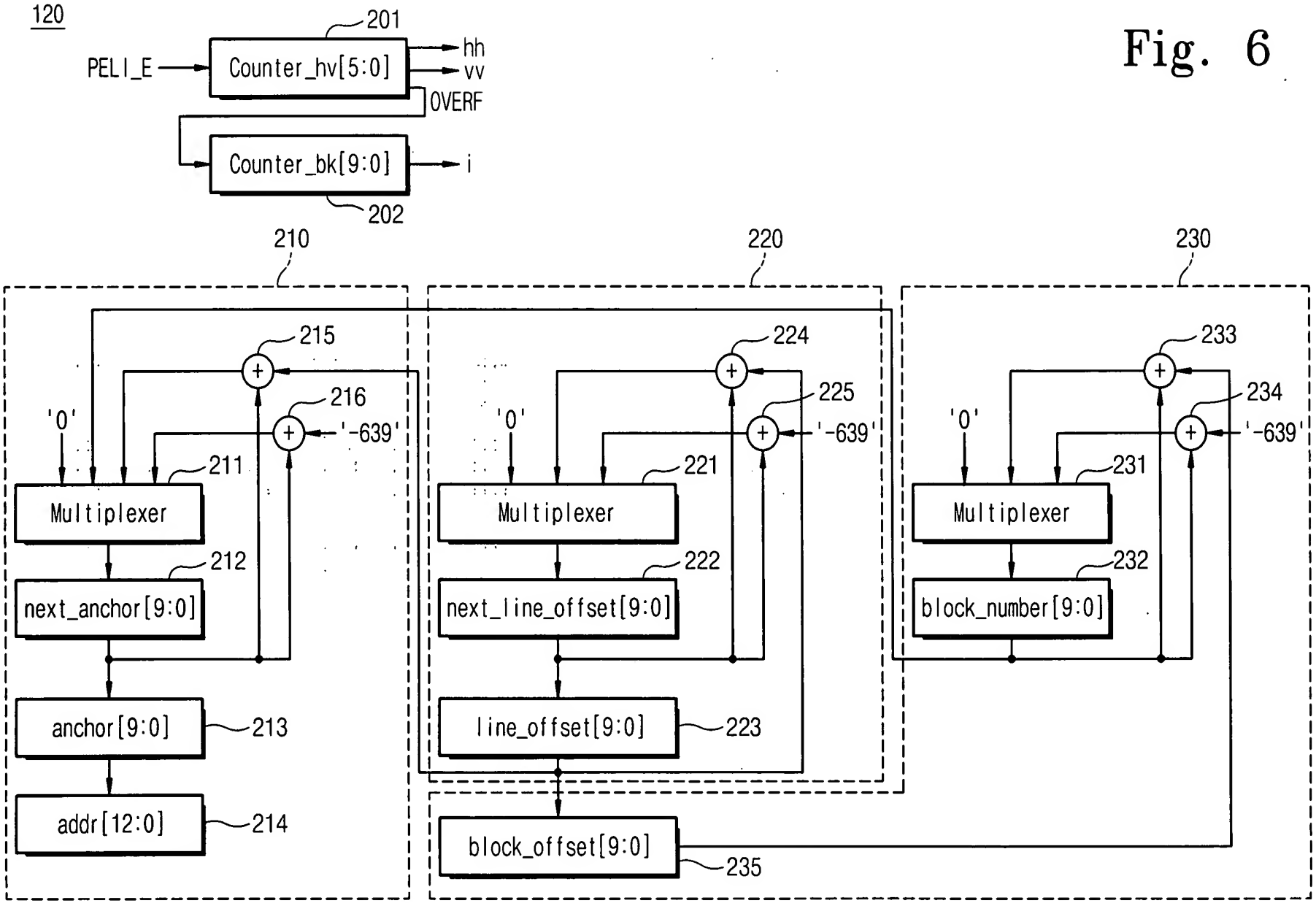
120
201
PELI_E
Counter_hv[5:0]
hh
vv
OVERF
Counter_bk[9:0]
i
202
210
220
230
215
216
'0'
'-639'
211
Multiplexer
212
next_anchor[9:0]
anchor[9:0]
213
addr[12:0]
214
224
225
'0'
'-639'
221
Multiplexer
222
next_line_offset[9:0]
line_offset[9:0]
223
233
234
'0'
'-639'
231
Multiplexer
232
block_number[9:0]
block_offset[9:0]
235

Fig. 7A

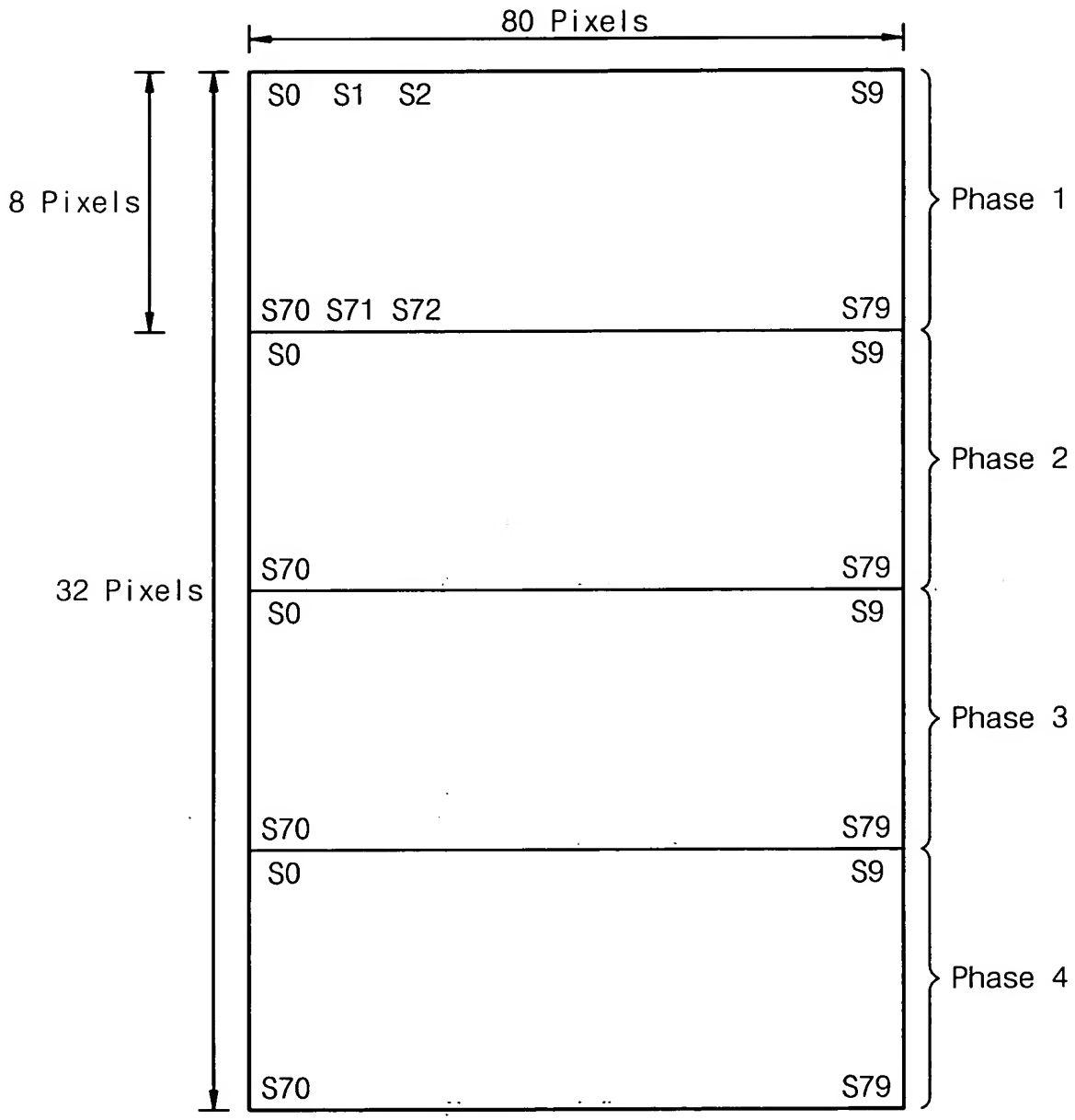
80 Pixels
8 Pixels
32 Pixels
S0 S1 S2
S9
S70 S71 S72
S79
S0
S9
S70
S79
S0
S9
S70
S79
S0
S9
S70
S79
Phase 1
Phase 2
Phase 3
Phase 4

Fig. 7B

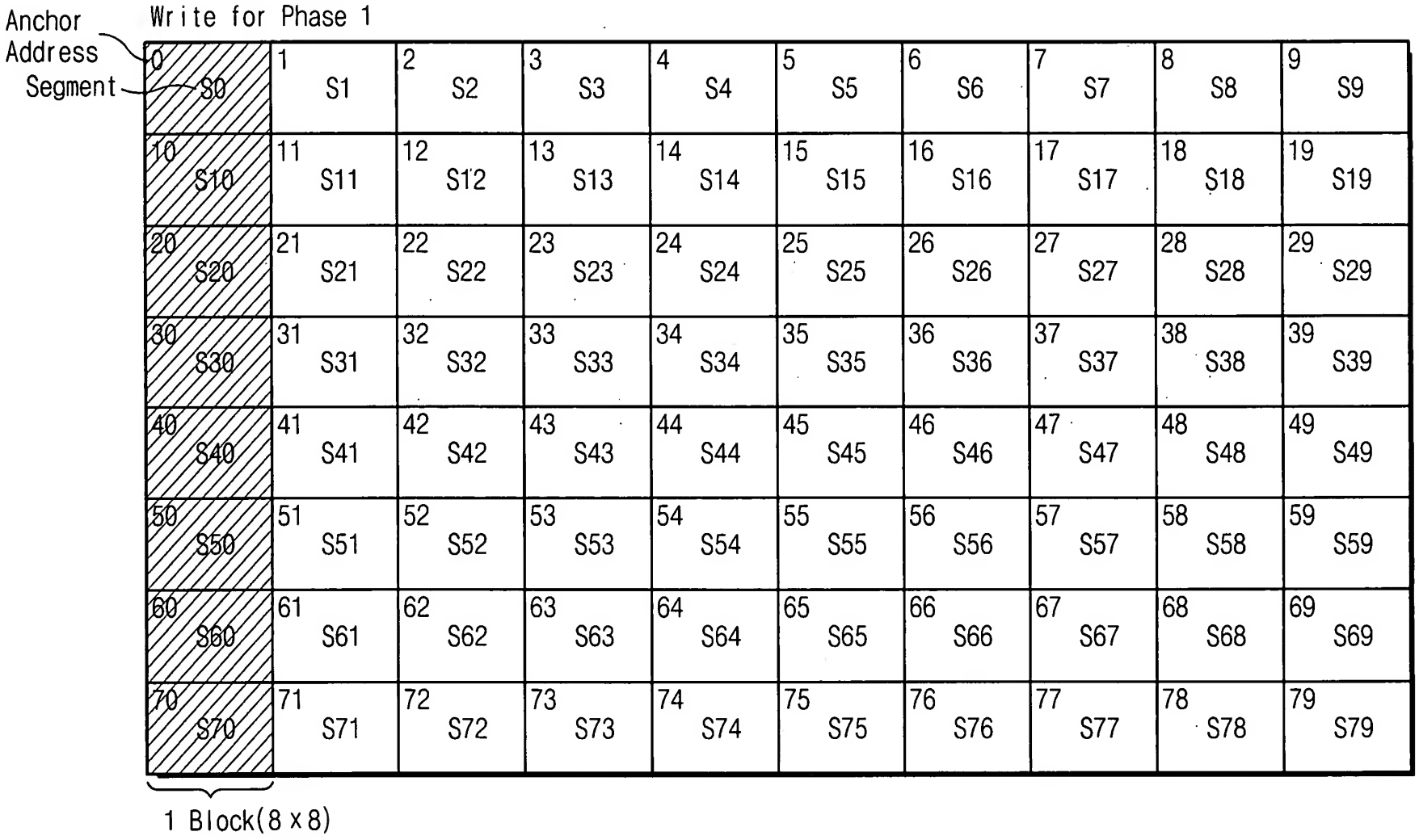
Anchor Address Segment
Write for Phase 1
0 S0
1 S1
2 S2
3 S3
4 S4
5 S5
6 S6
7 S7
8 S8
9 S9
10 S10
11 S11
12 S12
13 S13
14 S14
15 S15
16 S16
17 S17
18 S18
19 S19
20 S20
21 S21
22 S22
23 S23
24 S24
25 S25
26 S26
27 S27
28 S28
29 S29
30 S30
31 S31
32 S32
33 S33
34 S34
35 S35
36 S36
37 S37
38 S38
39 S39
40 S40
41 S41
42 S42
43 S43
44 S44
45 S45
46 S46
47 S47
48 S48
49 S49
50 S50
51 S51
52 S52
53 S53
54 S54
55 S55
56 S56
57 S57
58 S58
59 S59
60 S60
61 S61
62 S62
63 S63
64 S64
65 S65
66 S66
67 S67
68 S68
69 S69
70 S70
71 S71
72 S72
73 S73
74 S74
75 S75
76 S76
77 S77
78 S78
79 S79
1 Block(8 x 8)

Fig. 7C

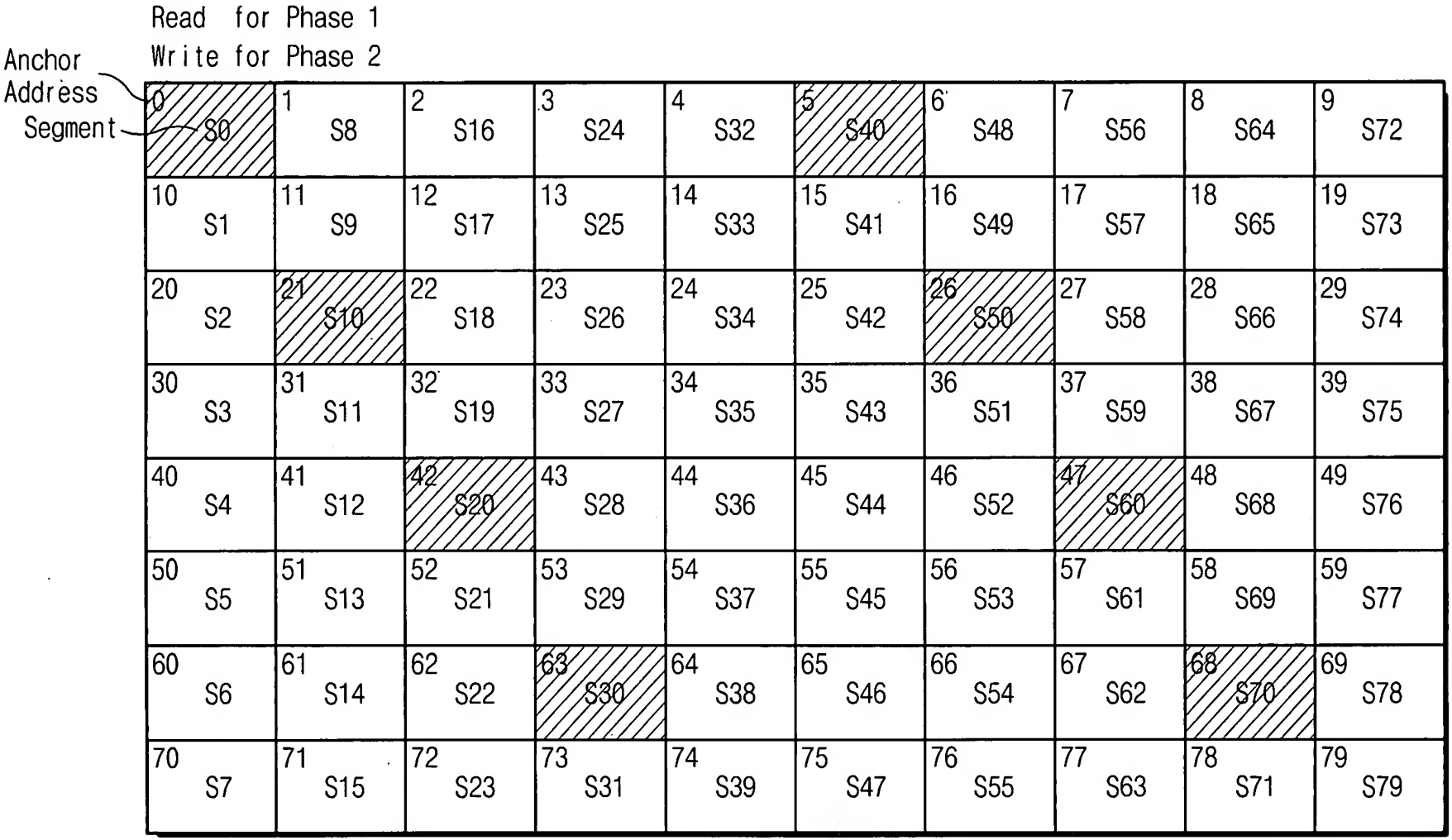
Read for Phase 1
Write for Phase 2
Anchor Address
Segment
0 S0
1 S8
2 S16
3 S24
4 S32
5 S40
6 S48
7 S56
8 S64
9 S72
10 S1
11 S9
12 S17
13 S25
14 S33
15 S41
16 S49
17 S57
18 S65
19 S73
20 S2
21 S10
22 S18
23 S26
24 S34
25 S42
26 S50
27 S58
28 S66
29 S74
30 S3
31 S11
32 S19
33 S27
34 S35
35 S43
36 S51
37 S59
38 S67
39 S75
40 S4
41 S12
42 S20
43 S28
44 S36
45 S44
46 S52
47 S60
48 S68
49 S76
50 S5
51 S13
52 S21
53 S29
54 S37
55 S45
56 S53
57 S61
58 S69
59 S77
60 S6
61 S14
62 S22
63 S30
64 S38
65 S46
66 S54
67 S62
68 S70
69 S78
70 S7
71 S15
72 S23
73 S31
74 S39
75 S47
76 S55
77 S63
78 S71
79 S79

Fig. 7D

Read for Phase 2
Write for Phase 3

Anchor Address Segment

0 S0	1 S64	2 S49	3 S34	4 S19	5 S4	6 S68	7 S53	8 S38	9 S23
10 S8	11 S72	12 S57	13 S42	14 S27	15 S12	16 S76	17 S61	18 S46	19 S31
20 S16	21 S1	22 S65	23 S50	24 S35	25 S20	26 S5	27 S69	28 S54	29 S39
30 S24	31 S9	32 S73	33 S58	34 S43	35 S28	36 S13	37 S77	38 S62	39 S47
40 S32	41 S17	42 S2	43 S66	44 S51	45 S36	46 S21	47 S6	48 S70	49 S55
50 S40	51 S25	52 S10	53 S74	54 S59	55 S44	56 S29	57 S14	58 S78	59 S63
60 S48	61 S33	62 S18	63 S3	64 S67	65 S52	66 S37	67 S22	68 S7	69 S71
70 S56	71 S41	72 S26	73 S11	74 S75	75 S60	76 S45	77 S30	78 S15	79 S79

Fig. 7E

Read for Phase 3
Write for Phase 4

Anchor Address Segment

0 S0	1 S38	2 S36	3 S35	4 S73	5 S32	6 S70	7 S29	8 S67	9 S26
10 S64	11 S23	12 S61	13 S20	14 S58	15 S17	16 S55	17 S14	18 S52	19 S11
20 S49	21 S8	22 S46	23 S5	24 S43	25 S2	26 S40	27 S78	28 S37	29 S75
30 S34	31 S72	32 S31	33 S69	34 S28	35 S66	36 S25	37 S63	38 S22	39 S60
40 S19	41 S57	42 S16	43 S54	44 S13	45 S51	46 S10	47 S48	48 S7	49 S45
50 S4	51 S42	52 S1	53 S39	54 S77	55 S36	56 S74	57 S33	58 S71	59 S30
60 S68	61 S27	62 S65	63 S24	64 S62	65 S21	66 S59	67 S18	68 S56	69 S15
70 S53	71 S12	72 S50	73 S9	74 S47	75 S6	76 S44	77 S3	78 S41	79 S79